The Art Of Analog Layout

A comprehensive and in-depth review of analog circuitlayout, schematic architecture, device, power network and ESDdesign This book will provide a balanced overview of analog circuitdesign layout, analog circuit schematic development,architecture of chips, and ESD design. It will start atan introductory level and will bring the reader right up to thestate-of-the-art. Two critical design aspects for analog and powerintegrated circuits are combined. The first design aspect coversanalog circuit design techniques to achieve the desired circuitperformance. The second and main aspect presents the additionalchallenges associated with the design of adequate and effective ESDprotection elements and schemes. A comprehensive list of practicalapplication examples is used to demonstrate the successfulcombination of both techniques and any potential designtrade-offs. Chapter One looks at analog design discipline, including layoutand analog matching and analog layout design practices. Chapter Twodiscusses analog design with circuits, examining: singletransistor amplifiers; multi-transistor amplifiers; active loadsand more. The third chapter covers analog design layout (alsoMOSFET layout), before Chapters Four and Five discuss analog designsynthesis. The next chapters introduce the

reader to analog-digitalmixed signal design synthesis, analog signal pin ESD networks, andanalog ESD power clamps. Chapter Nine, the last chapter, covers ESDdesign in analog applications. Clearly describes analog design fundamentals (circuitfundamentals) as well as outlining the various ESDimplications Covers a large breadth of subjects and technologies, such asCMOS, LDMOS, BCD, SOI, and thick body SOI Establishes an "ESD analog design" discipline thatdistinguishes itself from the alternative ESD digital designfocus Focuses on circuit and circuit design applications Assessible, with the artwork and tutorial style of the ESD bookseries PowerPoint slides are available for university facultymembers Even in the world of digital circuits, analog and power circuitsare two very important but under-addressed topics, especially fromthe ESD aspect. Dr. Voldman's new book will serve as anessential and practical guide to the greater IC community. Withhigh practical and academic values this book is a"bible" for professionals, graduate students, deviceand circuit designers for investigating the physics of ESD and forproduct designs and testing.

The modern economy is driven by technologies and knowledge. Digital technologies can free, shift and multiply choices, often intruding on the space of other industries, by providing new ways of conducting business operations and creating values for customers and companies. The topics covered in this volume

include software agents, multi-agent systems, agent modelling, mobile and cloud computing, big data analysis, business intelligence, artificial intelligence, social systems, computer embedded systems and nature inspired manufacturing, etc. that contribute to the modern Digital Economy. This volume highlights new trends and challenges in agent, new digital and knowledge economy research and includes 28 papers classified in the following specific topics: business process management, agent-based modeling and simulation, anthropic-oriented computing, learning paradigms, business informatics and gaming, digital economy, and advances in networked virtual enterprises. Published papers were selected for presentation at the 10th KES Conference on Agent and Multi-Agent Systems: Technologies and Applications (KES-AMSTA 2016) held in Puerto de la Cruz, Tenerife, Spain. Presented results would be of theoretical and practical value to researchers and industrial practitioners working in the fields of artificial intelligence, collective computational intelligence, innovative business models, new digital and knowledge economy and, in particular, agent and multi-agent systems, technologies, tools and applications.

This book presents an innovative methodology for the automatic generation of analog integrated circuits (ICs) layout, based on template descriptions and on evolutionary computational techniques. A design automation tool, LAYGEN II

was implemented to validate the proposed approach giving special emphasis to reusability of expert design knowledge and to efficiency on retargeting operations.

Covering the essentials of analog circuit design, this book takes a unique design approach based on a MOSFET model valid for all operating regions, rather than the standard square-law model. Opening chapters focus on device modeling, integrated circuit technology, and layout, whilst later chapters go on to cover noise and mismatch, and analysis and design of the basic building blocks of analog circuits, such as current mirrors, voltage references, voltage amplifiers, and operational amplifiers. An introduction to continuous-time filters is also provided, as are the basic principles of sampled-data circuits, especially switched-capacitor circuits. The final chapter then reviews MOSFET models and describes techniques to extract design parameters. With numerous design examples and exercises also included, this is ideal for students taking analog CMOS design courses and also for circuit designers who need to shorten the design cycle. This book introduces readers to a variety of tools for automatic analog integrated circuit (IC) sizing and optimization. The authors provide a historical perspective on the early methods proposed to tackle automatic analog circuit sizing, with emphasis on the methodologies to size and optimize the circuit, and on the

methodologies to estimate the circuit's performance. The discussion also includes robust circuit design and optimization and the most recent advances in layout-aware analog sizing approaches. The authors describe a methodology for an automatic flow for analog IC design, including details of the inputs and interfaces, multi-objective optimization techniques, and the enhancements made in the base implementation by using machine leaning techniques. The Gradient model is discussed in detail, along with the methods to include layout effects in the circuit sizing. The concepts and algorithms of all the modules are thoroughly described, enabling readers to reproduce the methodologies, improve the quality of their designs, or use them as starting point for a new tool. An extensive set of application examples is included to demonstrate the capabilities and features of the methodologies described.

Genetic Programming Theory and Practice III provides both researchers and industry professionals with the most recent developments in GP theory and practice by exploring the emerging interaction between theory and practice in the cutting-edge, machine learning method of Genetic Programming (GP). The contributions developed from a third workshop at the University of Michigan's Center for the Study of Complex Systems, where leading international genetic programming theorists from major universities and active practitioners from

leading industries and businesses meet to examine and challenge how GP theory informs practice and how GP practice impacts GP theory. Applications are from a wide range of domains, including chemical process control, informatics, and circuit design, to name a few.

This book constitutes the refereed proceedings of the 23st International Symposium on VLSI Design and Test, VDAT 2019, held in Indore, India, in July 2019. The 63 full papers were carefully reviewed and selected from 199 submissions. The papers are organized in topical sections named: analog and mixed signal design; computing architecture and security; hardware design and optimization; low power VLSI and memory design; device modelling; and hardware implementation.

This book introduces a design methodology that can help to bridge the productivity gap. Two different types of designs, depending on the design challenge, have been identified. To validate the presented methodologies, the authors have selected and designed accordingly three different industrial-strength applications.

This book tackles challenges for the design of analog integrated circuits that operate from ultra-low power supply voltages (down to 0.5V). Coverage demonstrates the signal processing circuit and circuit biasing approaches through the design of operational transconductance

amplifiers (OTAs). These amplifiers are then used to build analog system functions including continuous time filter and a sample and hold amplifier.

This book explains the application of recent advances in computational intelligence – algorithms, design methodologies, and synthesis techniques – to the design of integrated circuits and systems. It highlights new biasing and sizing approaches and optimization techniques and their application to the design of high-performance digital, VLSI, radio-frequency, and mixed-signal circuits and systems. This first of two related volumes addresses the design of analog and mixed-signal (AMS) and radio-frequency (RF) circuits, with 17 chapters grouped into parts on analog and mixed-signal applications, and radio-frequency design. It will be of interest to practitioners and researchers in computer science and electronics engineering engaged with the design of electronic circuits.

Circuit Design = Science + Art! Designers need a skilled "gut feeling" about circuits and related analytical techniques, plus creativity, to solve all problems and to adhere to the specifications, the written and the unwritten ones. You must anticipate a large number of influences, like temperature effects, supply voltages changes, offset voltages, layout parasitics, and numerous kinds of technology variations to end up with a circuit that works. This is challenging for analog, custom-digital, mixed-signal or RF circuits, and often researching new design methods in relevant journals, conference proceedings and design tools gives the impression unfortunately that just a "wild bunch" of "advanced techniques" exist. On the other hand, state-of-the-art tools nowadays indeed offer a good cockpit to steer the design flow, which include clever statistical methods and optimization techniques. Actually, this almost presents a second breakthrough, like the introduction of circuit simulators 40 years ago! Users

can now conveniently analyze all the problems (discover, quantify, verify), and even exploit them, for example for optimization purposes. Most designers are caught up on everyday problems, so we fit that "wild bunch" into a systematic approach for variation-aware design, a designer's field guide and more. That is where this book can help! Circuit Design: Anticipate, Analyze, Exploit Variations starts with best-practise manual methods and links them tightly to up-to-date automation algorithms. We provide many tractable examples and explain key techniques you have to know. We then enable you to select and setup suitable methods for each design task – knowing their prerequisites, advantages and, as too often overlooked, their limitations as well. The good thing with computers is that you yourself can often verify amazing things with little effort, and you can use software not only to your direct advantage in solving a specific problem, but also for becoming a better skilled, more experienced engineer. Unfortunately, EDA design environments are not good at all to learn about advanced numerics. So with this book we also provide two apps for learning about statistic and optimization directly with circuit-related examples, and in real-time so without the long simulation times. This helps to develop a healthy statistical gut feeling for circuit design. The book is written for engineers, students in engineering and CAD / methodology experts. Readers should have some background in standard design techniques like entering a design in a schematic capture and simulating it, and also know about major technology aspects.

Discover a fresh approach to efficient and insight-driven analog integrated circuit design in nanoscale-CMOS with this hands-on guide. Expert authors present a sizing methodology that employs SPICE-generated lookup tables, enabling close agreement between hand analysis and simulation. This enables the exploration of analog circuit tradeoffs using the gm/ID ratio as

a central variable in script-based design flows, and eliminates time-consuming iterations in a circuit simulator. Supported by downloadable MATLAB code, and including over forty detailed worked examples, this book will provide professional analog circuit designers, researchers, and graduate students with the theoretical know-how and practical tools needed to acquire a systematic and re-use oriented design style for analog integrated circuits in modern CMOS.

In the 11th edition in this successful series, the topics are structured-mixed-mode design, multi-bit sigma-delta converters and short range RF circuits. The book provides valuable information and excellent overviews of analogue circuit design, CAD and RF systems.

Analog circuit and system design today is more essential than ever before. With the growth of digital systems, wireless communications, complex industrial and automotive systems, designers are being challenged to develop sophisticated analog solutions. This comprehensive source book of circuit design solutions aids engineers with elegant and practical design techniques that focus on common analog challenges. The book's in-depth application examples provide insight into circuit design and application solutions that you can apply in today's demanding designs. This is the companion volume to the successful Analog Circuit Design: A Tutorial Guide to Applications and Solutions (October 2011), which has sold over 5000 copies in its the first 6 months of since publication. It extends the Linear Technology collection of application notes, which provides analog experts with a full collection of reference designs and problem solving insights to apply to their own engineering challenges Full support package including online resources (LTSpice) Contents include more application notes on power management, and data conversion and signal conditioning circuit solutions, plus an invaluable circuit collection of reference designs

CMOS short for complementary metal oxide semiconductor is widely used for designing high performance, low power integrated circuits for numerous applications. Basics of CMOS Cell Design introduces the design and simulation of CMOS integrated circuits in deep sub-micron technology. The book covers the MOS device, inverters, logic gates, arithmetics, interconnects and analog basic cells. A second book includes an extensive presentation of analog cells, radio-frequency analog blocks, analog to digital to analog converter principles, input/output interfacing silicon-insulator technology, and a discussion on future developments in microelectronics. The CD accompanying this book includes the lite 3 version of the PC tools MICROWIND and DSCH.

This book introduces readers to a variety of tools for analog layout design automation. After discussing the placement and routing problem in electronic design automation (EDA), the authors overview a variety of automatic layout generation tools, as well as the most recent advances in analog layout-aware circuit sizing. The discussion includes different methods for automatic placement (a template-based Placer and an optimization-based Placer), a fully-automatic Router and an empirical-based Parasitic Extractor. The concepts and algorithms of all the modules are thoroughly described, enabling readers to reproduce the methodologies, improve the quality of their designs, or use them as starting point for a new tool. All the methods described are applied to practical examples for a 130nm design process, as well as placement and routing benchmark sets.

Improving the performance of existing technologies has always been a focal practice in the development of computational systems. However, as circuitry is becoming more complex, conventional techniques are becoming outdated and new research

methodologies are being implemented by designers. Performance Optimization Techniques in Analog, Mix-Signal, and Radio-Frequency Circuit Design features recent advances in the engineering of integrated systems with prominence placed on methods for maximizing the functionality of these systems. This book emphasizes prospective trends in the field and is an essential reference source for researchers, practitioners, engineers, and technology designers interested in emerging research and techniques in the performance optimization of different circuit designs.

Verbal explanations are favored over mathematical formulas, graphs are kept to a minimum, and line drawings are used in this user-friendly book. Clear guidance and advice are provided for those professionals who lay out analog circuits. KEY TOPICS: Matching of resistors and capacitors: Includes causes of mismatch, particularly the hydrogen effect and package shift. MOS Transistors: Covers a brief history of floating gate devices, EPROM and EEPROM. Applications of MOS transistors: Expands information on failure mechanisms, including BVdss/Bvdii, SILC, NBTI/PTBI and GIDL and the difference between electrical and electrothermal SOA. Consideration of failure mechanisms as crucial to layout: Integrates further information into many chapters covering various devices. Standard bipolar, polygate CMOS and analog BiCMOS: Covers all three fundamental processes. MARKET: A valuable reference for professional layout designers.

As biosensors comprise a prospective alternative to traditional chemical analyses,

enabling fast on- and in-line measurements with sufficient selectivity, the field is expanding rapidly and is offering new ideas and developments every day. This book aims to cover the present state of the art in the biosensor technology and introduce the general aspects of biosensor- based techniques and methods. The book consists of 13 chapters by 44 authors and is divided into 3 sections, focused on bio-recognition techniques, signal transduction methods and signal analysis.

The tools and techniques you need to break the analog design bottleneck! Ten years ago, analog seemed to be a dead-end technology. Today, System-on-Chip (SoC) designs are increasingly mixed-signal designs. With the advent of application-specific integrated circuits (ASIC) technologies that can integrate both analog and digital functions on a single chip, analog has become more crucial than ever to the design process. Today, designers are moving beyond hand-crafted, one-transistor-at-a-time methods. They are using new circuit and physical synthesis tools to design practical analog circuits; new modeling and analysis tools to allow rapid exploration of system level alternatives; and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago. To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field, this volume collects in one place the essential set of analog CAD papers that form the foundation of today's new analog design automation tools. Areas covered are: Analog synthesis Symbolic analysis

Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer-Aided Design of Analog Integrated Circuits and Systems is the cutting-edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck.

As the frequency of communication systems increases and the dimensions of transistors are reduced, more and more stringent performance requirements are placed on analog circuits. This is a trend that is bound to continue for the foreseeable future and while it does, understanding performance trade-offs will constitute a vital part of the analog design process. It is the insight and intuition obtained from a fundamental understanding of performance conflicts and trade-offs, that ultimately provides the designer with the basic tools necessary for effective and creative analog design. Trade-offs in Analog Circuit Design, which is devoted to the understanding of trade-offs in analog design, is quite unique in that it draws together fundamental material from, and identifies interrelationships within, a number of key analog circuits. The book covers ten subject areas: Design methodology, Technology, General Performance, Filters, Switched Circuits, Oscillators, Data Converters, Transceivers, Neural Processing, and Analog CAD. Within these subject areas it deals with a wide diversity of trade-offs ranging from frequency-dynamic range and power, gain-bandwidth, speed-dynamic range and phase noise, to tradeoffs in design for manufacture and IC layout. The book

has by far transcended its original scope and has become both a designer's companion as well as a graduate textbook. An important feature of this book is that it promotes an intuitive approach to understanding analog circuits by explaining fundamental relationships and, in many cases, providing practical illustrative examples to demonstrate the inherent basic interrelationships and trade-offs. Trade-offs in Analog Circuit Design draws together 34 contributions from some of the world's most eminent analog circuits-and-systems designers to provide, for the first time, a comprehensive text devoted to a very important and timely approach to analog circuit design. The Art of Analog LayoutPrentice Hall

The microelectronics market, with special emphasis to the production of complex mixed-signal systems-on-chip (SoC), is driven by three main dynamics, time-- market, productivity and managing complexity. Pushed by the progress in na- meter technology, the design teams are facing a curve of complexity that grows exponentially, thereby slowing down the productivity design rate. Analog design automation tools are not developing at the same pace of technology, once custom design, characterized by decisions taken at each step of the analog design flow, - lies most of the time on designer knowledge and expertise. Actually, the use of - sign management platforms, like the Cadences Virtuoso platform, with a set of - tegrated CAD tools and database facilities to deal with the design transformations from the system level to the physical implementation, can significantly speed-up the design process and enhance the

productivity of analog/mixed-signal integrated circuit (IC) design teams. These design management platforms are a valuable help in analog IC design but they are still far behind the development stage of design automation tools already available for digital design. Therefore, the development of new CAD tools and design methodologies for analog and mixed-signal ICs is ess- tial to increase the designer's productivity and reduce design productivitygap. The work presented in this book describes a new design automation approach to the problem of sizing analog ICs.

"Electrostatic discharge (ESD)"--Page xxi.

An introduction to the design of analog VLSI circuits. Neuromorphic engineers work to improve the performance of artificial systems through the development of chips and systems that process information collectively using primarily analog circuits. This book presents the central concepts required for the creative and successful design of analog VLSI circuits. The discussion is weighted toward novel circuits that emulate natural signal processing. Unlike most circuits in commercial or industrial applications, these circuits operate mainly in the subthreshold or weak inversion region. Moreover, their functionality is not limited to linear operations, but also encompasses many interesting nonlinear operations similar to those occurring in natural systems. Topics include device physics, linear and nonlinear circuit forms, translinear circuits, photodetectors, floating-gate devices, noise analysis, and process technology.

This text addresses the design methodologies and CAD tools available for the systematic design and design automation of analogue integrated circuits. Two complementary approaches

discussed increase analogue design productivity, demonstrated throughout using design times of the different design experiments undertaken.

This book covers modern analog components, their characteristics, and interactions with process parameters. It serves as a comprehensive guide, addressing both the theoretical and practical aspects of modern silicon devices and the relationship between their electrical properties and processing conditions. Based on the authors' extensive experience in the development of analog devices, this book is intended for engineers and scientists in semiconductor research, development and manufacturing. The problems at the end of each chapter and the numerous charts, figures and tables also make it appropriate for use as a text in graduate and advanced undergraduate courses in electrical engineering and materials science. Enables engineers to understand analog device physics, and discusses important relations between process integration, device design, component characteristics, and reliability; Describes in step-by-step fashion the components that are used in analog designs, the particular characteristics of analog components, while comparing them to digital applications; Explains the second-order effects in analog devices, and trade-offs between these effects when designing components and developing an integrated process for their manufacturing.

It is a great honor to provide a few words of introduction for Dr. Georges Gielen's and Prof. Willy Sansen's book "Symbolic analysis for automated design of analog integrated circuits". The symbolic analysis method presented in this book represents a significant step forward in the area of analog circuit design. As demonstrated in this book, symbolic analysis opens up new possibilities for the development of computer-aided design (CAD) tools that can analyze

an analog circuit topology and automatically size the components for a given set of specifications. Symbolic analysis even has the potential to improve the training of young analog circuit designers and to guide more experienced designers through second-order phenomena such as distortion. This book can also serve as an excellent reference for researchers in the analog circuit design area and creators of CAD tools, as it provides a comprehensive overview and comparison of various approaches for analog circuit design automation and an extensive bibliography. The world is essentially analog in nature, hence most electronic systems involve both analog and digital circuitry. As the number of transistors that can be integrated on a single integrated circuit (IC) substrate steadily increases over time, an ever increasing number of systems will be implemented with one, or a few, very complex ICs because of their lower production costs.

A practical and comprehensive reference that explores Electrostatic Discharge (ESD) in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems. Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection. Written by a noted expert on the topic, the text offers a topic-by-topic reference that includes illustrative figures, discussions, and drawings. The handbook covers a wide-range of topics including ESD in manufacturing (garments, wrist straps, and shoes); ESD Testing; ESD device physics; ESD semiconductor process effects; ESD failure mechanisms; ESD circuits in different technologies (CMOS, Bipolar, etc.); ESD circuit types (Pin, Power, Pin-to-Pin, etc.); and much more. In addition, the text includes a glossary, index,

tables, illustrations, and a variety of case studies. Contains a well-organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians, operators, engineers, circuit designers, and failure analysis engineers, The ESD Handbook contains an accessible reference to ESD design and ESD systems.

This book examines the issue of design of fully-integrated frequency synthesizers suitable for system-on-a-chip (SOC) processors. This book takes a more global design perspective in jointly examining the design space at the circuit level as well as at the architectural level. The coverage of the book is comprehensive and includes summary chapters on circuit theory as well as feedback control theory relevant to the operation of phase locked loops (PLLs). On the circuit level, the discussion includes low-voltage analog design in deep submicron digital CMOS processes, effects of supply noise, substrate noise, as well device noise. On the architectural level, the discussion includes PLL analysis using continuous-time as well as discrete-time models, linear and nonlinear effects of PLL performance, and detailed analysis of locking behavior. The material then develops into detailed circuit and architectural analysis of specific clock generation blocks. This includes circuits and architectures of PLLs with high power supply noise immunity and digital PLL architectures where the loop filter is digitized. Methods of generating low-spurious sampling clocks for discrete-time analog blocks are then examined. This includes sigma-delta fractional-N PLLs, Direct Digital Synthesis (DDS) techniques and non-conventional uses of PLLs. Design for test (DFT) issues as they arise in

PLLs are then discussed. This includes methods of accurately measuring jitter and built-in-self-test (BIST) techniques for PLLs. Finally, clocking issues commonly associated to system-on-a-chip (SOC) designs, such as multiple clock domain interfacing and partitioning, and accurate clock phase generation techniques using delay-locked loops (DLLs) are also addressed. The book provides numerous real world applications, as well as practical rules-of-thumb for modern designers to use at the system, architectural, as well as the circuit level. This book is well suited for practitioners as well as graduate level students who wish to learn more about time-domain analysis and design of frequency synthesis techniques.

This book covers the fundamental knowledge of layout design from the ground up, addressing both physical design, as generally applied to digital circuits, and analog layout. Such knowledge provides the critical awareness and insights a layout designer must possess to convert a structural description produced during circuit design into the physical layout used for IC/PCB fabrication. The book introduces the technological know-how to transform silicon into functional devices, to understand the technology for which a layout is targeted (Chap. 2). Using this core technology knowledge as the foundation, subsequent chapters delve deeper into specific constraints and aspects of physical design, such as interfaces, design rules and libraries (Chap. 3), design flows and models (Chap. 4), design steps (Chap. 5), analog design specifics (Chap. 6), and finally reliability measures (Chap. 7). Besides serving as a textbook for engineering students, this book is a foundational reference for today's circuit designers.

This book describes new tools for front end analog designers, starting with global variation-aware sizing, and extending to novel variation-aware topology design. The tools aid design through automation, but more importantly, they also aid designer insight through automation.

We now describe four design tasks, each more general than the previous, and how this book contributes design aids and insight aids to each. The ?rst designer task targeted is global robust sizing. This task is supported by a design tool that does automated, globally reliable, variation-aware s- ing (SANGRIA),and an insight-aiding tool that extracts designer-interpretable whitebox models that relate sizings to circuit performance (CAFFEINE). SANGRIA searches on several levels of problem dif?culty simultaneously, from lower cheap-to-evaluate "exploration" layers to higher full-evaluation "exploitation" layers (structural homotopy). SANGRIAmakes maximal use of circuit simulations by performing scalable data mining on simulation results to choose new candidate designs. CAFFEINE accomplishes its task by tre- ing function induction as a tree-search problem. It constrains its tree search space via a canonical-functional-form grammar, and searches the space with grammatically constrained genetic programming. The second designer task is topology selection/topology design. Topology selection tools must consider a broad variety of topologies such that an app-priate topology is selected, must easily adapt to new semiconductor process nodes, and readily incorporate new topologies. Topology design tools must allow designers to creatively explore new topology ideas as rapidly as possible.

Jarenlang probeerde Ryder Carroll steeds weer nieuwe productiviteitsmethodes, zowel online als offline, maar niets werkte zoals hij wilde. Uit pure wanhoop ontwikkelde hij zijn eigen systeem, de Bullet Journal Methode, die hem hielp om zich beter te concentreren en productief te zijn. Hij deelde zijn methode met enkele vrienden die dezelfde uitdagingen tegenkwamen, en voor hij het wist had hij een viral beweging in gang gezet. We zijn nu een paar jaar verder, en Bullet Journaling vindt inmiddels wereldwijd navolging. De Bullet Journal Methode behelst

zoveel meer dan aantekeningen organiseren en lijstjes maken. Het gaat over wat Carroll 'leven met intentie' noemt: afleidingen leren negeren en je tijd en energie richten op de dingen die er echt toe doen, zowel in je werk als in je persoonlijke leven. Dit boek leert je... Het verleden vastleggen: Creëer een duidelijk en uitgebreid overzicht van je gedachten, met niets meer dan pen en papier. Het heden organiseren: Vind dagelijks rust door je takenlijst op een bewuste, systematische en productieve manier aan te pakken. De toekomst plannen: Zet interesses en losse aantekeningen om in zinvolle doelen en verdeel die vervolgens in hanteerbare actiestappen die tot grote veranderingen leiden. Ryder Carroll schreef dit boek voor vastgelopen lijstjesmakers, overweldigde multitaskers en creatievelingen die structuur nodig hebben. Of je nu al jarenlang een Bullet Journal gebruikt of er nog nooit een hebt gezien, De Bullet Journal Methode helpt je om het stuur van je leven weer in eigen handen te nemen. A indústria eletrônica tem apresentado uma demanda crescente pela fabricação de aparelhos onde o baixo consumo de energia é uma das características mais importantes. Como exemplo, temos os telefones celulares, os computadores pessoais portáteis e os implantes biomédicos. Este trabalho investiga o projeto e o layout de células analógicas de consumo mil vezes menos (micropower) que os circuitos convencionais. As células desenvolvidas tanto podem ser usadas em aplicações analógicas quanto em circuitos híbridos formados por blocos digitais e blocos analógicos em um mesmo circuito integrado (mixed-mode).O trabalho desenvolvido envolveu 7 etapas principais: o estudo da operação do transistor MOS polarizado na região de inversão fraca comparado com a região de inversão forte; o estudo de estruturas básicas com dois transitores operando na inversão fraca; a conversão dos parâmetros de fabricante para a simulação das células; estudo de células analógicas a e seu

projeto para baixo consumo; simulação das células e comparação com células comerciais; estudo da variação dos parâmetros de fabricação; estudo de técnicas de layout para células analógicas. Inicialmente o trabalho apresenta um resumo do estado da arte em projetos de circuitos integrados analógicos CMOS e, introduz o conceito da operação do transistor MOS em inversão fraca (weak inversion).O estudo de estruturas básicas, tais como espelhos de corrente, é o passo seguinte para a compreensão das limitações da operação dos transistores na fraca inversão e a análise de suas vantagens e desvantagens. A conversão dos parâmetros de processos fornecido pelo fabricante, do SPICE nível 2 para o SMASH nível 5, é um passo importante para uma simulação mais fiel do transistor real operando na região de inversão fraca, usando o novo modelo EKV (desenvolvido pela Escola Politécnica Federal de Lausanne - EPFL).O desenvolvimento dos blocos funcionais analógicas, tais como amplificadores operacionais, tece como estratégia de trabalho partir de especificações de células existentes em bibliotecas de fabricantes comerciais com tecnologia reconhecida sobre o assunto, e tentar reproduzir as suas características através do projeto de células dedicadas. Foram avaliadas algumas topologias de uma mesma célula com o objetivo de realizar a comparação entre elas. As medidas de desempenho das células para a comparação com as comerciais, foram realizadas com o uso de arquivos hierárquicos de simulação, visando a redução da quantidade de arquivos. Foi realizado um estudo de como a variação do processo de fabricação pode afetar o desempenho das células projetadas por análise de Montecarlo. São mostradas técnicas de layout de células analógicas que visam reduzir o descasamento entre transistores, faro este que poderia levar o circuito a apresentar comportamento diferente daquele especificado inicialmente. Os resultados alcançados demonstraram ser possível o

desenvolvimento de células analógicas de baixo consumo. Através do uso da técnica de operação do transistor na região de inversão fraca, obteve-se desempenho comparável aos circuitos comerciais, tornando possível a criação de uma biblioteca de células analógicas mais ampla sem a necessidade da dependência do know-how dos fabricantes comerciais.

The exploration of the subnuclear world is done through increasingly complex experiments covering a wide range of energies and in a large variety of environments OCo from particle accelerators and underground detectors to satellites and space laboratories. For these research programs to succeed, novel techniques, new materials and new instrumentation need to be used in detectors, often on a large scale. Hence, particle physics is at the forefront of technological advancement and leads to numerous applications. Among these, medical applications have a particular importance due to the health and social benefits they bring. This volume reviews the advances made in all technological aspects of current experiments in the field."

Analog integrated circuits are very important as interfaces between the digital parts of integrated electronic systems and the outside world. A large portion of the effort involved in designing these circuits is spent in the layout phase. Whereas the physical design of digital circuits is automated to a large extent, the layout of analog circuits is still a manual, time-consuming and error-prone task. This is mainly due to the continuous nature of analog signals, which causes analog circuit performance to be very sensitive to layout parasitics. The parasitic elements associated with interconnect wires cause loading and coupling effects that degrade the frequency behaviour and the noise performance of analog circuits. Device mismatch and thermal effects put a fundamental limit on the achievable accuracy of circuits. For successful

automation of analog layout, advanced place and route tools that can handle these critical parasitics are required. In the past, automatic analog layout tools tried to optimize the layout without quantifying the performance degradation introduced by layout parasitics. Therefore, it was not guaranteed that the resulting layout met the specifications and one or more layout iterations could be needed. In Analog Layout Generation for Performance and Manufacturability, the authors propose a performance driven layout strategy to overcome this problem. In this methodology, the layout tools are driven by performance constraints, such that the final layout, with parasitic effects, still satisfies the specifications of the circuit. The performance degradation associated with an intermediate layout solution is evaluated at runtime using predetermined sensitivities. In contrast with other performance driven layout methodologies, the tools proposed in this book operate directly on the performance constraints, without an intermediate parasitic constraint generation step. This approach makes a complete and sensible trade-off between the different layout alternatives possible at runtime and therefore eliminates the possible feedback route between constraint derivation, placement and layout extraction. Besides its influence on the performance, layout also has a profound impact on the yield and testability of an analog circuit. In Analog Layout Generation for Performance and Manufacturability, the authors outline a new criterion to quantify the detectability of a fault and combine this with a yield model to evaluate the testability of an integrated circuit layout. They then integrate this technique with their performance driven routing algorithm to produce layouts that have optimal manufacturability while still meeting their performance specifications. Analog Layout Generation for Performance and Manufacturability will be of interest to analog engineers, researchers and students.

Environmental electromagnetic pollution has drastically increased over the last decades. The omnipresence of communication systems, various electronic appliances and the use of ever increasing frequencies, all contribute to a noisy electromagnetic environment which acts detrimentally on sensitive electronic equipment. Integrated circuits must be able to operate satisfactorily while cohabiting harmoniously in the same appliance, and not generate intolerable levels of electromagnetic emission, while maintaining a sound immunity to potential electromagnetic disturbances: analog integrated circuits are in particular more easily disturbed than their digital counterparts, since they don't have the benefit of dealing with predefined levels ensuring an innate immunity to disturbances. The objective of the research domain presented in EMC of Analog Integrated Circuits is to improve the electromagnetic immunity of considered analog integrated circuits, so that they start to fail at relevantly higher conduction levels than before.

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